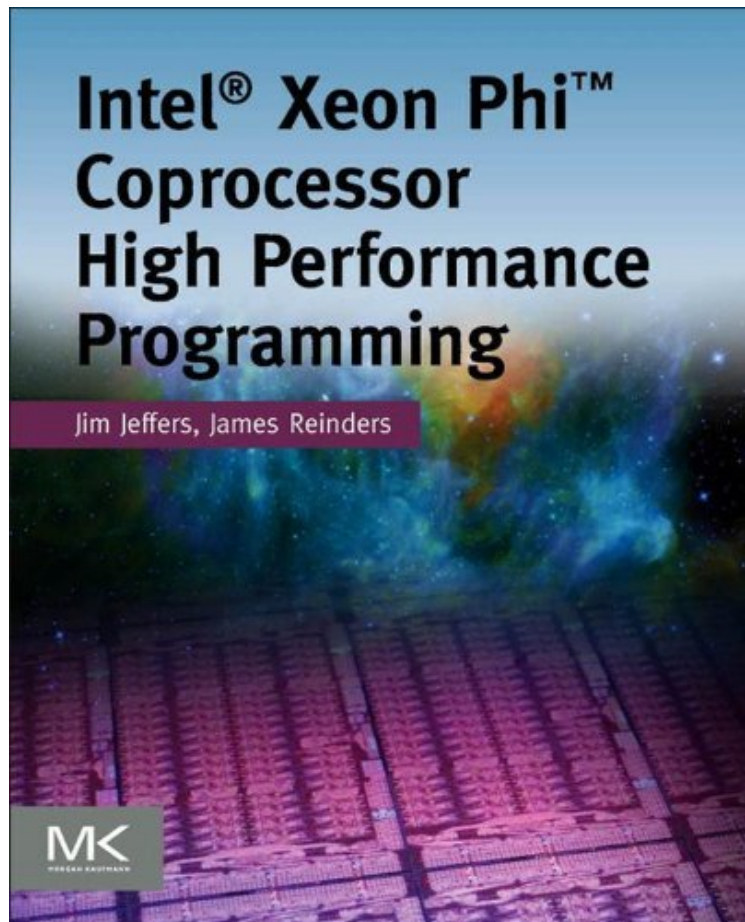


[Pdf free] Intel Xeon Phi Coprocessor High Performance Programming

# Intel Xeon Phi Coprocessor High Performance Programming

Von James Jeffers, James Reinders  
ebooks | Download PDF | \*ePub | DOC | audiobook



DOWNLOAD



READ ONLINE

Produktinformation - Verkaufsrang: #809158 in eBooks Veröffentlicht am: 2013-02-11 Erscheinungsdatum: 2013-02-11 File Name: B00BWYOAA4 | File size: 16.Mb

**Von James Jeffers, James Reinders : Intel Xeon Phi Coprocessor High Performance Programming** before purchasing it in order to gauge whether or not it would be worth my time, and all praised Intel Xeon Phi Coprocessor High Performance Programming:

Kundenrezensionen  
Hilfreichste Kundenrezensionen  
0 von 0 Kunden fanden die folgende Rezension hilfreich. Guter Einstieg  
Von Dr. rer. nat. Michael Burger  
Das Buch von Reinders und Jeffers bietet einen allgemeinen Einstieg in die Xeon Phi Programmierung bzw. das Programmieren von Beschleunigern. Nach einem Ein- und Überblick über die Xeon Phi Hard- und Software folgen anhand simpler Beispiele Erläuterungen und Strategien für Thread-Parallelisierung und Vektorisierung. Diese Kapitel sind für jeden Programmierer interessant, da sie auch auf normalen Desktop- und Serverprozessoren zu effizienterem Code führen. Die Kapitel 6 und 7 behandeln mit Alignment und Offload-Programmierung Phi-spezifischere Themen, die sehr ausführlich besprochen und anhand weiterer Beispiele veranschaulicht werden. Die letzten Kapitel im Buch geben dann tiefere Einblicke in Hardware- und Softwareumgebung des Beschleunigers, sowie reihen kurz einige andere relevante Themen wie MPI, Libraries und Performanceanalyse auf dem Phi an. Dieses Anreihen geschieht meiner Meinung nach aber zu kurz, weshalb ich auch

den einen Stern abziehe. Da dies das erste und lange Zeit einzige Buch über den Xeon Phi war, hätte ich mir her etwas Tiefgang gewünscht, da Anfang 2013 die Informationsmenge über den Phi doch sehr gering war und somit viel durch Ausprobieren erarbeitet werden musste. 0 von 0 Kunden fanden die folgende Rezension hilfreich. Guter Einstieg zur Programmierung des Xeon Phi. Von Kassiem Jacobs Das Buch ist erstklassig geeignet zum Einstieg in die Programmierung des Xeon Phi. Die Beispielprogramme und ihre Funktionsweise sind gut beschrieben und verständlich beschrieben. Wenn man den Xeon Phi operationell einsetzen will und ggf. Software portieren oder neu schreiben will/muss, wird man nicht kommen sich auch konzeptionell mit parallelem Programmieren (Methoden) und parallelen Algorithmen auseinander zu setzen. 1 von 2 Kunden fanden die folgende Rezension hilfreich. Intel Phi Von Bernhard Oestlinger Ein im Grunde gelungenes Buch ... was mich noch mehr interessiert hatte, warum kein Standardprogramm für die Phi erhältlich ist! Eine politische Entscheidung der Hersteller der Software. Mit der Phi wird manches Programm extrem viel besser, besser als mit der Cuda-Technik. Ich hoffe für die Zukunft, dass die Phi sich so richtig durchsetzen wird, und das nicht nur im Experimentellen.

**Kurzbeschreibung** Authors Jim Jeffers and James Reinders spent two years helping educate customers about the prototype and pre-production hardware before Intel introduced the first Intel Xeon Phi coprocessor. They have distilled their own experiences coupled with insights from many expert customers, Intel Field Engineers, Application Engineers and Technical Consulting Engineers, to create this authoritative first book on the essentials of programming for this new architecture and these new products. This book is useful even before you ever touch a system with an Intel Xeon Phi coprocessor. To ensure that your applications run at maximum efficiency, the authors emphasize key techniques for programming any modern parallel computing system whether based on Intel Xeon processors, Intel Xeon Phi coprocessors, or other high performance microprocessors. Applying these techniques will generally increase your program performance on any system, and better prepare you for Intel Xeon Phi coprocessors and the Intel MIC architecture. A practical guide to the essentials of the Intel Xeon Phi coprocessor Presents best practices for portable, high-performance computing and a familiar and proven threaded, scalar-vector programming model Includes simple but informative code examples that explain the unique aspects of this new highly parallel and high performance computational product Covers wide vectors, many cores, many threads and high bandwidth cache/memory architecture **Pressestimmen** This book belongs on the bookshelf of every HPC professional. Not only does it successfully and accessibly teach us how to use and obtain high performance on the Intel MIC architecture, it is about much more than that. It takes us back to the universal fundamentals of high-performance computing including how to think and reason about the performance of algorithms mapped to modern architectures, and it puts into your hands powerful tools that will be useful for years to come. -Robert J. Harrison, Institute for Advanced Computational Science, Stony Brook University, from the Foreword ""This book belongs on the bookshelf of every HPC professional. Not only does it successfully and accessibly teach us how to use and obtain high performance on the Intel MIC architecture, it is about much more than that. It takes us back to the universal fundamentals of high-performance computing including how to think and reason about the performance of algorithms mapped to modern architectures, and it puts into your hands powerful tools that will be useful for years to come."" -Robert J. Harrison, Institute for Advanced Computational Science, Stony Brook University, from the Foreword "Reinders and Jeffers have written an outstanding book about much more than the Intel(r) Xeon Phi . This is a comprehensive overview of the challenges in realizing the performance potential of advanced architectures, including modern multi-core processors and many-core coprocessors. The authors provide a cogent explanation of the reasons why applications often fall short of theoretical performance, and include steps that application developers can take to bridge the gap. This will be recommended reading for all of my staff." James A. Ang, Ph.D. Senior Manager, Extreme-scale Computing, Sandia National Laboratories "The authors consummate knowledge of the architecture shines through in this excellent introduction to the fundamentals of programming for the Intel(r) Xeon Phi coprocessor." I highly recommend this engaging treatise to programmers interested in effectively utilizing the Intel(r) Xeon Phi coprocessor." R. Glenn Brook, Ph.D., Chief Technology Officer, Joint Institute for Computational Sciences, Director, Application Acceleration Center of Excellence, University of Tennessee / Oak Ridge National Laboratory The authors have provided a very readable, big-picture introduction to programming the Intel Xeon Phi Coprocessor. By chronicling step-by-step optimizations of several computational kernels, software interfaces are illustrated for getting the most out of key architectural features of the Intel Xeon Phi Coprocessor." James L. Schwarzmeier, Cray Inc, January 2013. "This book belongs on the bookshelf of every HPC professional. Not only does it successfully and accessibly teach us how to use and obtain high performance on the Intel MIC architecture, it is about much more than that. It takes us back to the universal fundamentals of high-performance computing including how to think and reason about the performance of algorithms mapped to modern architectures, and it puts into your hands powerful tools that will be useful for years to come." Robert J. Harrison, Institute for Advanced Computational Science, Stony Brook University, from the Foreword ""Reinders and Jeffers have written an outstanding book about much more than the Intel(R) Xeon Phi(TM).

This is a comprehensive overview of the challenges in realizing the performance potential of advanced architectures, including modern multi-core processors and many-core coprocessors. The authors provide a cogent explanation of the reasons why applications often fall short of theoretical performance, and include steps that application developers can take to bridge the gap. This will be recommended reading for all of my staff." --James A. Ang, Ph.D. Senior Manager, Extreme-scale Computing, Sandia National Laboratories "The authors' consummate knowledge of the architecture shines through in this excellent introduction to the fundamentals of programming for the Intel(R) Xeon Phi(TM) coprocessor." I highly recommend this engaging treatise to programmers interested in effectively utilizing the Intel(R) Xeon Phi(TM) coprocessor." --R. Glenn Brook, Ph.D., Chief Technology Officer, Joint Institute for Computational Sciences, Director, Application Acceleration Center of Excellence, University of Tennessee / Oak Ridge National Laboratory "The authors have provided a very readable, big-picture introduction to programming the Intel Xeon Phi Coprocessor. By chronicling step-by-step optimizations of several computational kernels, software interfaces are illustrated for getting the most out of key architectural features of the Intel Xeon Phi Coprocessor." --James L. Schwarzmeier, Cray Inc, January 2013." "This book belongs on the bookshelf of every HPC professional. Not only does it successfully and accessibly teach us how to use and obtain high performance on the Intel MIC architecture, it is about much more than that. It takes us back to the universal fundamentals of high-performance computing including how to think and reason about the performance of algorithms mapped to modern architectures, and it puts into your hands powerful tools that will be useful for years to come." --Robert J. Harrison, Institute for Advanced Computational Science, Stony Brook University, from the Foreword-Reinders and Jeffers have written an outstanding book about much more than the Intel(R) Xeon Phi(TM). This is a comprehensive overview of the challenges in realizing the performance potential of advanced architectures, including modern multi-core processors and many-core coprocessors. The authors provide a cogent explanation of the reasons why applications often fall short of theoretical performance, and include steps that application developers can take to bridge the gap. This will be recommended reading for all of my staff.- --James A. Ang, Ph.D. Senior Manager, Extreme-scale Computing, Sandia National Laboratories -The authors' consummate knowledge of the architecture shines through in this excellent introduction to the fundamentals of programming for the Intel(R) Xeon Phi(TM) coprocessor.- I highly recommend this engaging treatise to programmers interested in effectively utilizing the Intel(R) Xeon Phi(TM) coprocessor.- --R. Glenn Brook, Ph.D., Chief Technology Officer, Joint Institute for Computational Sciences, Director, Application Acceleration Center of Excellence, University of Tennessee / Oak Ridge National Laboratory -The authors have provided a very readable, big-picture introduction to programming the Intel Xeon Phi Coprocessor. By chronicling step-by-step optimizations of several computational kernels, software interfaces are illustrated for getting the most out of key architectural features of the Intel Xeon Phi Coprocessor.- --James L. Schwarzmeier, Cray Inc, January 2013.- -This book belongs on the bookshelf of every HPC professional. Not only does it successfully and accessibly teach us how to use and obtain high performance on the Intel MIC architecture, it is about much more than that. It takes us back to the universal fundamentals of high-performance computing including how to think and reason about the performance of algorithms mapped to modern architectures, and it puts into your hands powerful tools that will be useful for years to come.- -- Robert J. Harrison, Institute for Advanced Computational Science, Stony Brook University, from the Foreword

**Kurzbeschreibung** Authors Jim Jeffers and James Reinders spent two years helping educate customers about the prototype and pre-production hardware before Intel introduced the first Intel Xeon Phi coprocessor. They have distilled their own experiences coupled with insights from many expert customers, Intel Field Engineers, Application Engineers and Technical Consulting Engineers, to create this authoritative first book on the essentials of programming for this new architecture and these new products. This book is useful even before you ever touch a system with an Intel Xeon Phi coprocessor. To ensure that your applications run at maximum efficiency, the authors emphasize key techniques for programming any modern parallel computing system whether based on Intel Xeon processors, Intel Xeon Phi coprocessors, or other high performance microprocessors. Applying these techniques will generally increase your program performance on any system, and better prepare you for Intel Xeon Phi coprocessors and the Intel MIC architecture. A practical guide to the essentials of the Intel Xeon Phi coprocessor Presents best practices for portable, high-performance computing and a familiar and proven threaded, scalar-vector programming model Includes simple but informative code examples that explain the unique aspects of this new highly parallel and high performance computational product Covers wide vectors, many cores, many threads and high bandwidth cache/memory architecture